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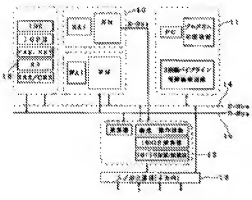
(54) DIGITAL ARRAY PROCESSOR BEING EXCLUSIVE TO MULTI-DATA TYPE NEURAL NETWORK OF MULTI-COMMAND AND SYSTEM CONSTITUTED BY USING THE PROCESSOR



(57)Abstract:
PROBLEM TO BE SOLVED: To effectively simulate a neural network model by permitting a system to have the structure of a unique arithmetic equipment, a memory, a communication port and a program memory which are suitable for the numeral model.
SOLUTION: The system is composed of the four blocks of the memory and a general purpose register block 10, the program memory and a control block 11, an arithmetic equipment block 12 and a communication block 13. Then, bus (BUS) is separated into the one 14 for a program and the one 15 for data. The operation of a processor is executed by following the command set in the program memory. The command can easily simulate the neural network and the configuration of the command decides the hardware structure of the processor. Therefore, the hardware (chip) for simulating the nural network model by using the VLSI technique of a present digital system is stably produced.

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[Detailed Description of the Invention]

[0001] **[Field of the Invention]** In the digital processor design for which this invention used the art of VLSI (Very Large Scale Integration), It is related with the embodiment of the processor only for a nerve net of the data multiplex type of a multiplex instruction word, i.e., an MIMD (Multiple Insruction stream, Multiple Data stream) mold, or the parallel processor only for a nerve net.

[0002] **[Description of the Prior Art]** Catching up in research of a nerve net (neural network) is looking for a model similar to the identification method in an organism.

[0003]For this reason, research which led the mathematical modeling using biological analysis and this simulation besides biological research is done.

[0004]However, in order to carry out a simulation, a high-speed computer is required.

[0005]Since a long time will be consumed, in order to obtain an expected result, considerable patience is required for the simulation using the existing computer.

[0006]Then, research of the hardware which can carry out the simulation of the nerve net model specially is advancing.

[0007]This is not only a stage of a laboratory, but has the system actually used regularly.

[0008]In such an embodiment method, we embody hardware using digital VLSI art applicable at a present stage.

[0009]Drawing 6 is structural drawing of the error back propagation model in the neural model used considerably now.

[0010]This model consists of a course operation of a forward direction, and a course operation of an opposite direction.

[0011]In M1 of the 2nd layer called one nerve cell, the multiplication of the input value (NK) and weightings (WK1) which come from the 1st layer is carried out, and the basic motion of a forward direction course will be again outputted as an input value of the 3rd layer through a nonlinear function, if what doubled the result goes into the nerve cell M1.

[0012]Even the 3rd [at least] layer, the same operation is carried out and a result comes out as an output.

[0013]Operation of an opposite direction course is also similar to a front thing.

[0014]As writing of relation, there are "Parallel Distributed Processing, Vol.l, David E Rumelhart, et al, and A Bradford Book Company."

[0015]When the feature of this model is seen, I hear that there are much of it being a model of parallel operation and data (the multiplication of an input value and weightings and operation of these doubling) which must be processed, and there is.

[0016]Then, the simulation of the nerve net model can be suddenly carried out also for the system which can perform parallel operation effectively.

[0017]The digital method and the analog method are one of the embodiment methods which used the electronic method in the method of embodying the system of a nerve net.

[0018]However, if it embodies as the analog method using the present art, the degree of location is good, but a system is not stabilized but the method of making it learn becomes difficult.

[0019]Although the embodiment using the digital method has a low degree of location, the problem the outside of it is solved fairly.

[0020]Then, it is easy for the embodiment using the digital method to apply from a actual problem as the present art.

[0021]For this reason, although various methods are proposed, there is an appropriate problem.

[0022]Therefore, an object of this invention is to provide the thing in which the digital array processor only for a nerve net of the MIMID type with the structure which can carry out the simulation of the nerve net model which needs considerable data processing promptly effectively was formed on the VLSI chip.

[0023]It comprises said processor and the purpose is in providing a system with the optimal structure.

[0024] **[Means for Solving the Problem]** This invention did not raise performance of a particular part of conventional technology, and a VLSI chip with an original structure is designed.

[0025]A processor is designed for the purpose of deviating from structure of a general-purpose microprocessor and carrying out a nerve net model.

[0026]There is a memory in an inside of a processor and the memory structure can perform a simulation of a nerve net model now easily.

[0027]A data path mist beam simulation of structure of a computing unit and an inside can be easily performed now.

[0028]It is easy for communication of interprocessor of a parallel processor to carry out the simulation of the nerve net model by improving an existing handshaking method.

[0029] **[Embodiment of the Invention]** Hereafter, with reference to an attached drawing, the embodiment of this invention is described in detail.

[0030]Drawing 1 is structural drawing of the whole array processor which is one embodiment of this invention, and comprises a memory and the general-purpose register block 10, program memory and the control block 11, the computing unit block 12, and four blocks of the communication block 13.

[0031]And bus (BUS) is divided into 14 for a program, and 15 for data.

[0032]Operation of a processor is carried out as the instruction word set as program memory.

[0033]The instruction word (command) is what can carry out the simulation of the nerve net model easily, and the composition of an instruction word determines the hardware structure of a processor.

[0034]Drawing 2 is structural drawing of the computing unit which constitutes the array processor which is one embodiment of this invention.

[0035]The numerals WM are one in the data which comes from a weightings memory, the data as for which XM comes from input memories, and the data in which ACC comes in the output of an accumulator and, as for rfo, a general-purpose register's output and IO come from the communication port of four directions.

[0036]AC and AV are carry and an overflow flag, respectively, and AN/AZ/AP is a flag with which the value of an accumulation machine shows a negative number / zero / positive number.

[0037]In relation to drawing 2, the computing unit comprises the two-step pipeline parallel-parallel multiplier 20, the parallel adder/subtractor 21, the logic machine 22 and the accumulator 23, and the flag register 24.

[0038]The register 25 for data emergency storage and MUX for data selections are included.

[0039]The feature of said computing unit carries out pipeline operation, and took [for this reason] two fields into consideration.

[0040]The first, it is the side of hardware structure.

[0041]The multiplier is carrying out two-step pipeline operation, and is connected with an adding machine/subtractor, and series, and carries out three-stage pipeline operation.

[0042]It is supply of the data for the second pipeline operation.

[0043]Two separated memories are used for continuous data supply.

[0044]The memory (WM) 30 with weightings important for a nerve net model and the memory (XM) 31 with an input value are separated.

[0045]If the processor has weightings from the beginning of study and the recognition stage where the operation of a nerve net model is performed, they are advantageous.

[0046]However, since the input value must enter continuously from the outside from a recognition process, the processor does not need to have it, but it is advantageous that the processor has at the time of study.

[0047]The data path chose the shortest course as much as possible in consideration of working speed, and equalized the course of the data which flows out of a processor.

[0048]For this reason, a logic circuit is placed out of an accumulator, and IO value which comes from the outside flows only through the shortest possible course, and it is made to go.

[0049]Drawing 3 shows the memory block.

[0050]There are two independent memories and the general-purpose register is displayed only on drawing 1.

[0051]In carrying out the simulation of the nerve net, a general-purpose register is a very important portion.

[0052]Although the nerve net is using simple arithmetic models, if a program is actually created, a specific variable needs to be used repetitive.

[0053]The performance of a processor can be raised if a general-purpose register is used for repetitive use of such a variable.

[0054]There are eight memory pointer registers in the weightings memory 30.

[0055]If the simulation of the nerve net model is carried out, some continuous memory addresses will have accomplished the group and such a group will be repeatedly used rather than calling it continuous use of a memory.

[0056]Then, many pointer registers 32 are certainly required for the weightings memory 30.

[0057]And the computing unit 34 for calculating an address is also required.

[0058]Although the memory 31 with an input value may have the address pointer 33 of the number smaller than weightings, many address pointers are required for it too.

[0059]And a memory can be effectively used only by there being the increase machine 35 for calculating an address.

[0060]The composition (WM, XM) from which the memory was separated is required because of the pipeline operation of an operation.

[0061]And in order to solve the phenomenon of the head of a communicative bottle of opting for the performance of a parallel processor, if possible, the internal memory of large capacity is effective.

[0062]The register 37 stores an address temporarily, and from the exterior of an array processor, in data, the address bus 38 is used a rise / in order to carry out downloading.

[0063]Drawing 4 is structural drawing of the communication port by this invention, and comprises the register 46 who specifies beforehand the port for outputting and inputting the input port block 40, the output port block 41, and data.

[0064]Said input port block 40 comprises MUX44 which chooses and receives data from one in four data at the time of the buffer 42 for the flag (IRS) 47 which displays a state for an input, and data storage, and data input.

[0065]Said output port block 41 comprises DEMUX45 which chooses data, in order to send data to one buffer in four data buffers at the time of the buffer 43 for the flag (ORS) 48 which displays a state for an output, and data storage, and data output.

[0066]In the embodiment of this invention, it communicates using the handshaking method.

[0067]The processor is communicating in the four directions and communication is performed in the one direction at once in four directions.
[0068]In the embodiment of this invention, since such a communication direction is used for the register 46, appointing it beforehand, quick communication can carry out.

[0069]Drawing 5 is one example of the system which can be constituted using the designed processor.

[0070]Since the processor is carrying out communication of four directions, the optimal structure is a two-dimensional (2-Dimension) gestalt.

[0071]It can also have the structure of the parallel system of other gestalten.

[0072]And since the connection circuit 52 is placed if required, it can have the external memory 34.

[0073]In order to connect with the host computer 53, the connection circuit 51 is needed.

[0074]Since the address bus 56 is an one way, the address has been sent to the one way from the host computer 53, and since the data bus 55 is a bidirectional bus, bidirectional data exchange is possible for it.

[0075]There is an effect which can manufacture stably the hardware (chip) for carrying out the simulation of the nerve net model by the embodiment of this invention which is constituted as mentioned above and operates using the VLSI art of the present digital system.

[0076]The simulation of the various nerve net models can be carried out using the digital system in which a program is possible.

[0077]It can be adopted as a processing element to a parallel system, the embodiment as a large-scale parallel system which connected hundreds of chips partly is possible for the designed chip, and can connect some chips and can use them also for the dedicated system of the specific purpose.

[0078] **[Effect of the Invention]** Since said chip has the structure of the original computing unit which suited the nerve net model, a memory, a communication port, and program memory, the simulation of the nerve net model can be carried out effectively.

CLAIMS

[Claim(s)]

[Claim 1]In a digital array processor using VLSI technology only for a nerve net, A memory and a general-purpose register block (10) with a memory configuration (WM, XM) separated for pipeline operation of an operation, A computing unit block (12) which is provided with a program memory and control-block (11) two-step pipeline parallel-parallel multiplier (20), a parallel adder/subtractor (21), a logic machine (22), and an accumulator (23), is constituted, and carries out various kinds of required operations, And four blocks of a communication block (13) for communication of interprocessor, And an MIMD [which having the bus (BUS) of a form divided into a bus for data (15) for transmitting a rise / bus for a program for carrying out downloading (14), and data in a program, and constituting] type digital array processor only for a nerve net.

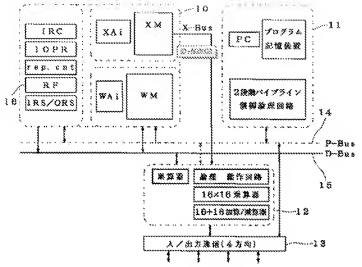
[Claim 2]A two-step pipeline parallel-parallel multiplier (20) with which said computing unit block (12) calculates multiplication, A logic machine (22) which performs addition, the parallel adder/subtractor (21) and a logical operation which calculate subtraction, and an operation relevant to this, A flag register (24) for storing an accumulator (23) which stores a result of an operation again, and a carry flag (AC), an overflow flag (AV) and a flag (AN/AZ/AP) with which a value of an accumulator shows a negative number / zero / positive number, A provided with MUX for register (25) and data selections (26) for storing data temporarily MIMD [according to claim 1] type digital array processor only for a nerve net.

[Claim 3]An according to claim 1 MIMD [the multiplier's (20)'s carrying out two step pipeline operation of said computing unit block (12), connecting with an adding machine/subtractor, and series, and performing pipeline operation of a three-stage] type digital array processor only for a nerve net.

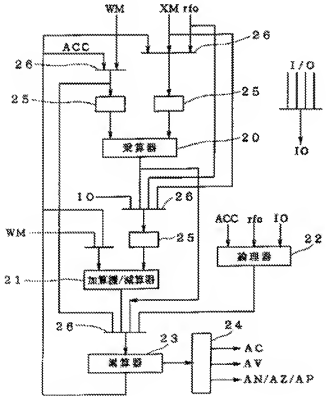
[Claim 4]Said computing unit block (12) for continuous data supply, A digital array processor

according to claim 3 MIMD type [with a memory of structure which separated a memory (XM) with a memory (WM) with weightings important for a nerve net model, (30), and an input value, and (31)] only for a nerve net.
[Claim 5]A data path of said computing unit block (12), In order to equalize a course of data which chooses the shortest course as much as possible, and flows and goes out of a processor, An according to claim 4 MIMD [, wherein IO value which places a logic machine (22) out of an accumulator (23), and comes from the outside is constituted so that it may flow only through the shortest possible course and may go] type digital array processor only for a nerve net.
[Claim 6]Said memory and a general-purpose register block (10), A general-purpose register who is used for repetitive use of a variable and raises performance of a processor, Many pointer registers (32) for specifying sRAM (30) for storing weightings, and a group of a continuous memory address, A weightings memory (WM) constituted by having a register (37) for storing an adding machine (34) for calculating an address, and an address temporarily, Many pointer registers (33) for specifying sRAM (31) for storing an input value, and a group of a continuous memory address, An input value memory (XM) constituted by having a register (37) for storing an increase machine (35) for calculating an address, and an address temporarily, And an according to claim 1 MIMD [having a rise / address bus (38) for carrying out downloading for data from the exterior of an array processor] type digital array processor only for a nerve net.
[Claim 7]A flag (IRS) (47) with which said communication block (13) displays a state for an input, An input port block (40) containing MUX (44) which chooses and receives one data in four data at the time of a buffer (42) for data storage, and data input, An output port block (41) containing DEMUX (45) chosen in order to send data to one buffer in four data buffers at the time of a buffer (43) for a flag (ORS) (48) which displays a state for an output, and data storage, and data output, And a provided with register (46) who specifies port for outputting and inputting data beforehand MIMD [according to claim 1] type digital array processor only for a nerve net.
[Claim 8]An according to claim 1 MIMD [which is characterized by quick communication being possible since said processor communicates in the four directions, and a communication direction is used for a register (46) in four directions, appointing it beforehand] type digital array processor only for a nerve net.
[Claim 9]In a system provided with a digital array processor only for a nerve net, Claim 1 arranged by two-dimensional form thru/or Claim 8 either Said processor (50) of a description, A connection circuit (51) for connecting with a host computer (53), A connection circuit (52) for connecting an external memory (54), A system using an MIMD [which having an address bus (56) for sending an address to an one way, and comprising a bidirectional data bus (55) in which data exchange is possible and a host computer (53)] type digital array processor only for a nerve net.

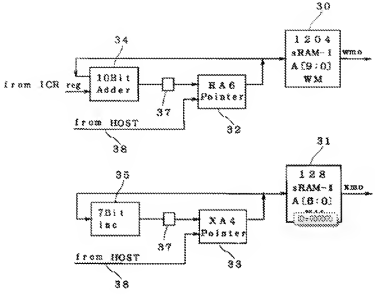
[Drawing 1]



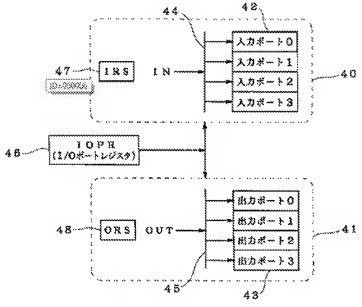
[Drawing 2]



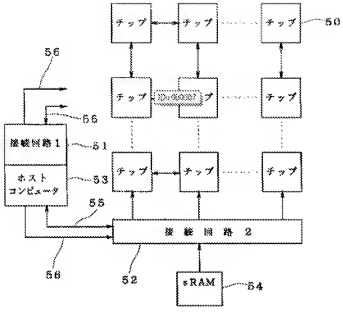
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Drawing 6]